

FIG. 1 is a block diagram of a wireless communication device 100. The device 100 includes a programmable logic device die 106, a base band unit 108, an RF transceiver 110, an amplifier 112, and an antenna 104. The programmable logic device die 106 is connected to the base band unit 108. The base band unit 108 is connected to the RF transceiver 110. The RF transceiver 110 is connected to the amplifier 112. The amplifier 112 is connected to the antenna 104. The base band unit 108, RF transceiver 110, and amplifier 112 are enclosed in a dashed box 114. The antenna 104 is connected to the device 100 via a feed line 102.

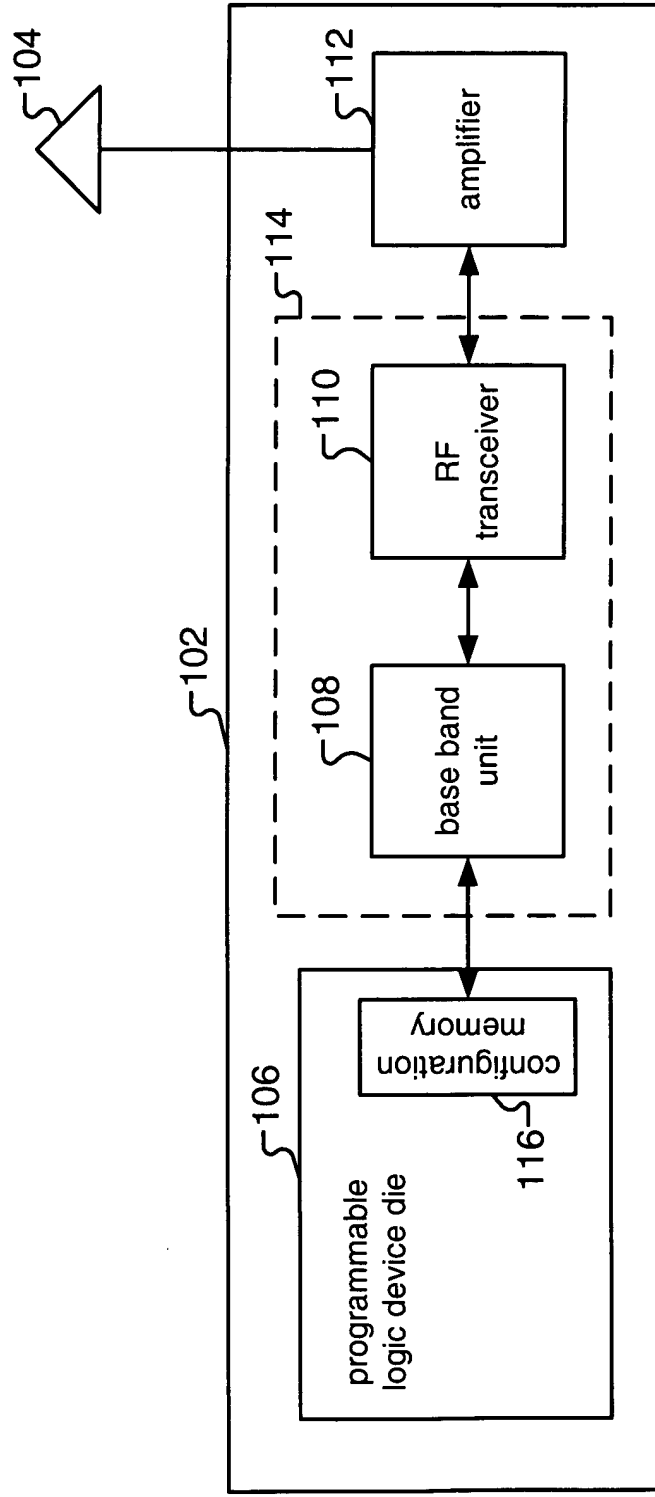


FIG. 1

FIG. 2 is a block diagram of a system 130. The system 130 includes a host 132, an antenna 134, and a device 136. The device 136 includes an IC 141, an IC 139, an FPGA 142, and an IC 140. The device 136 is connected to the host 132 via a connection 133. The antenna 134 is connected to the host 132 via a connection 135.

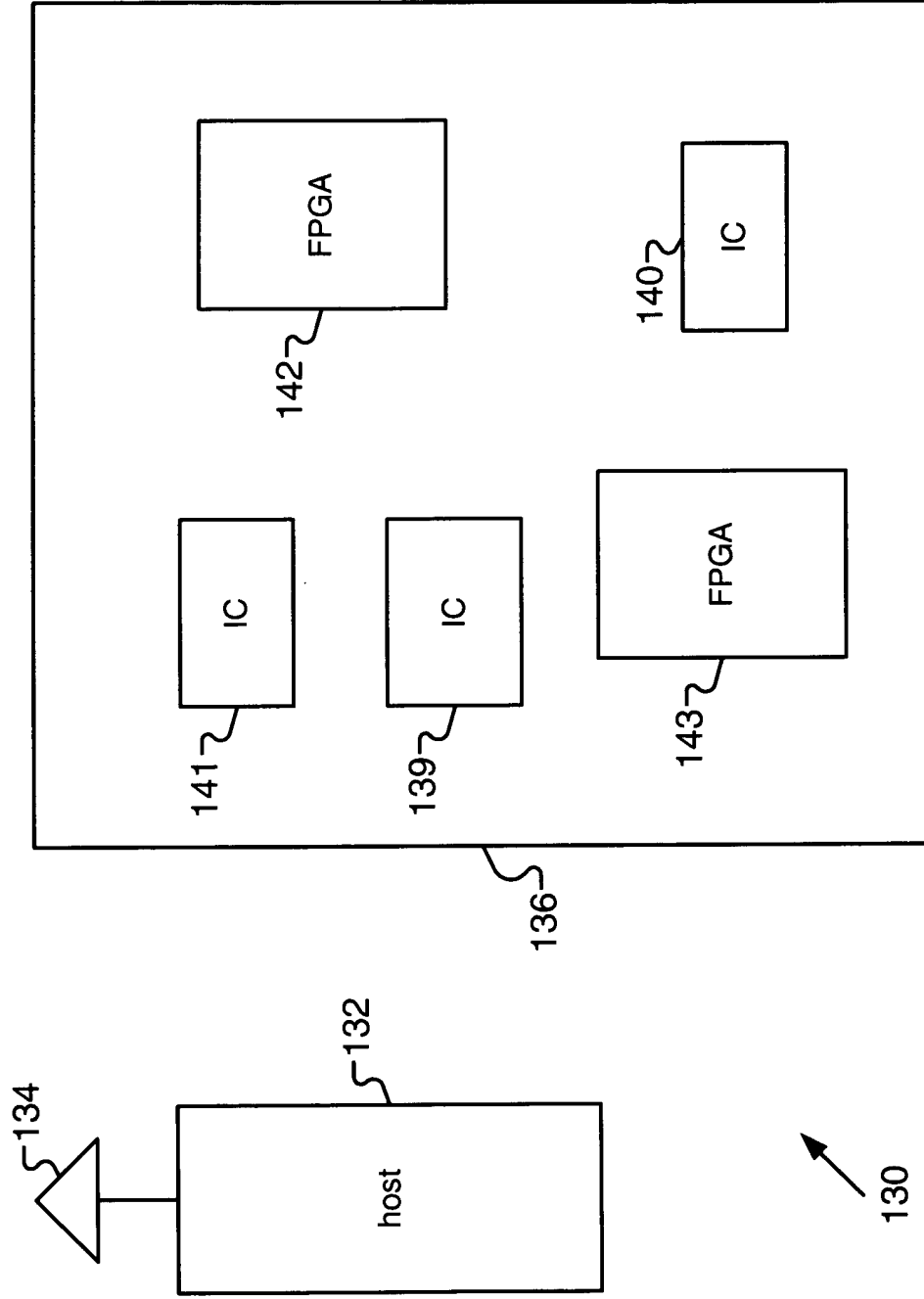


FIG. 2

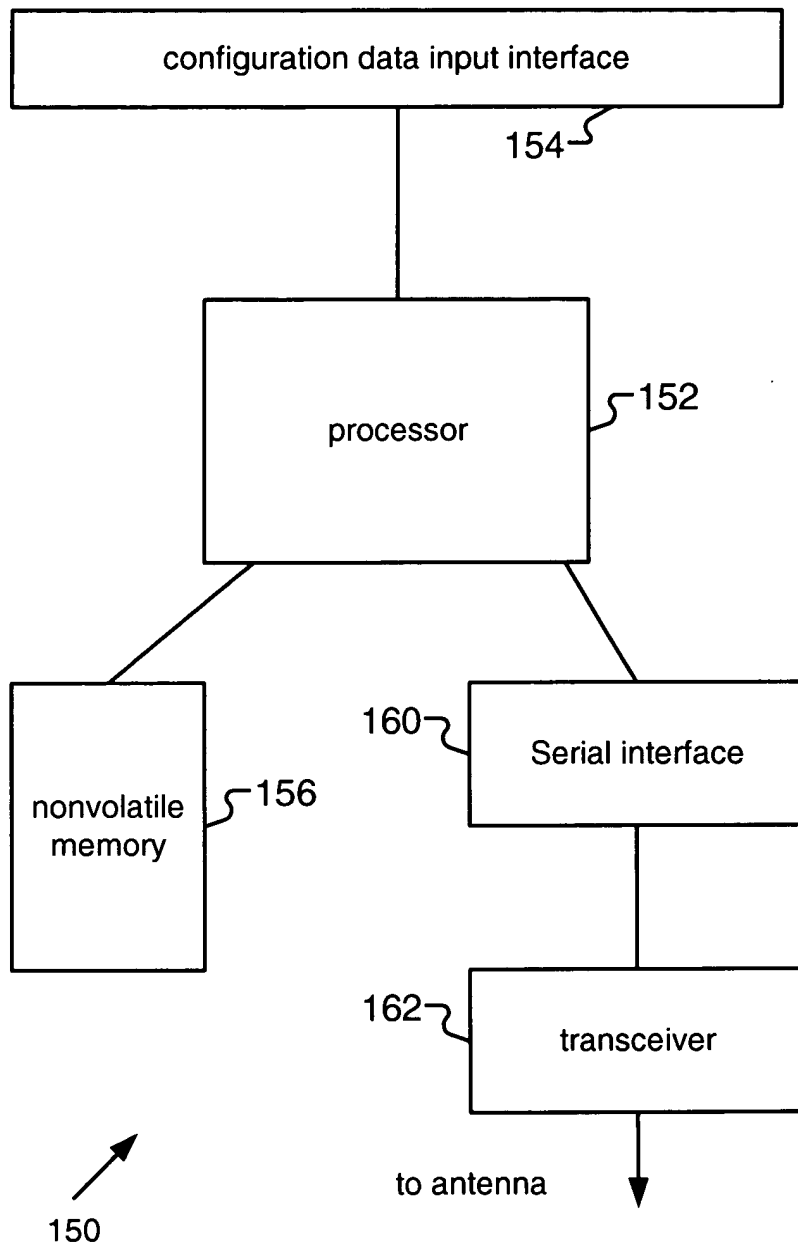


FIG. 3

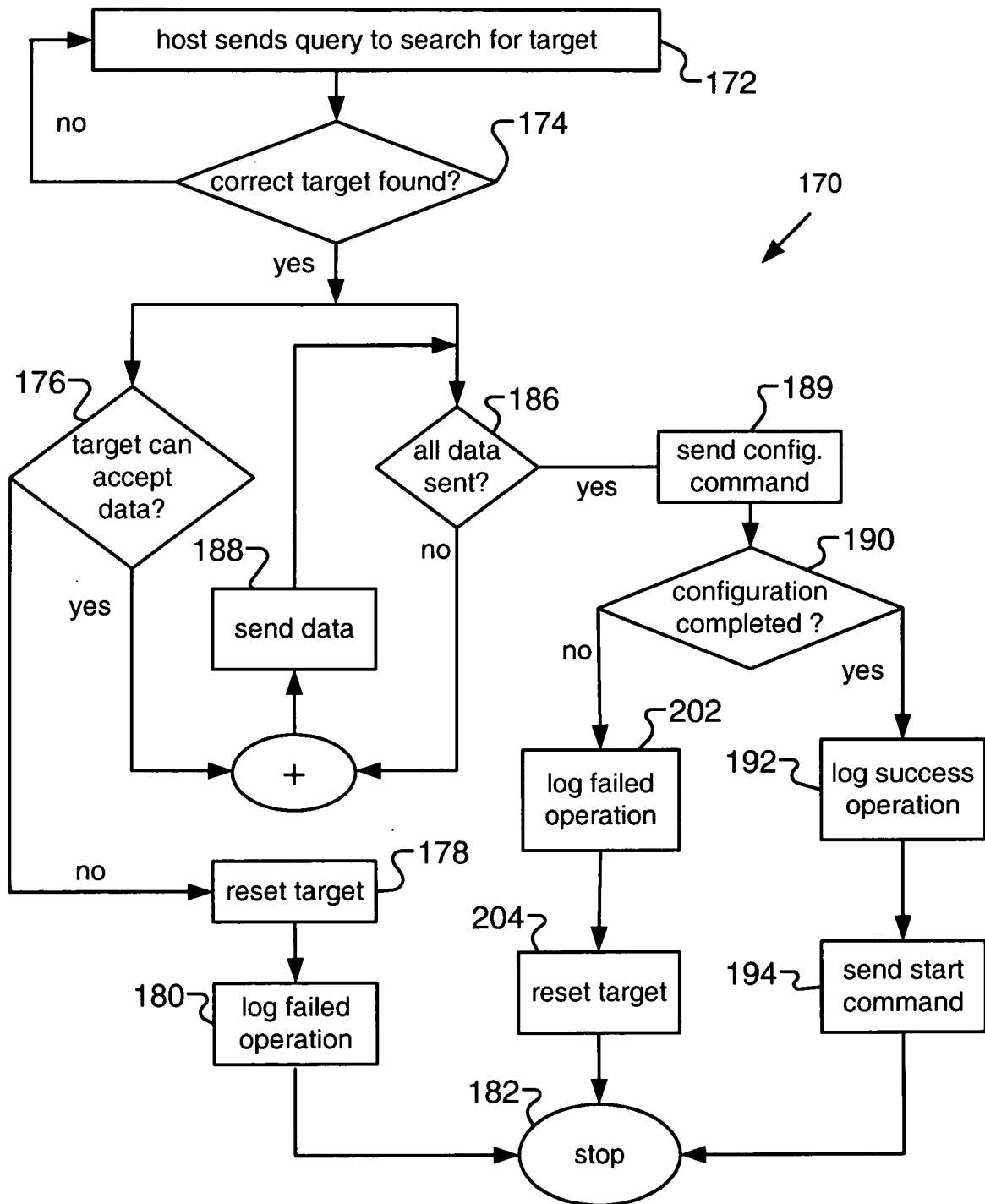


FIG. 4

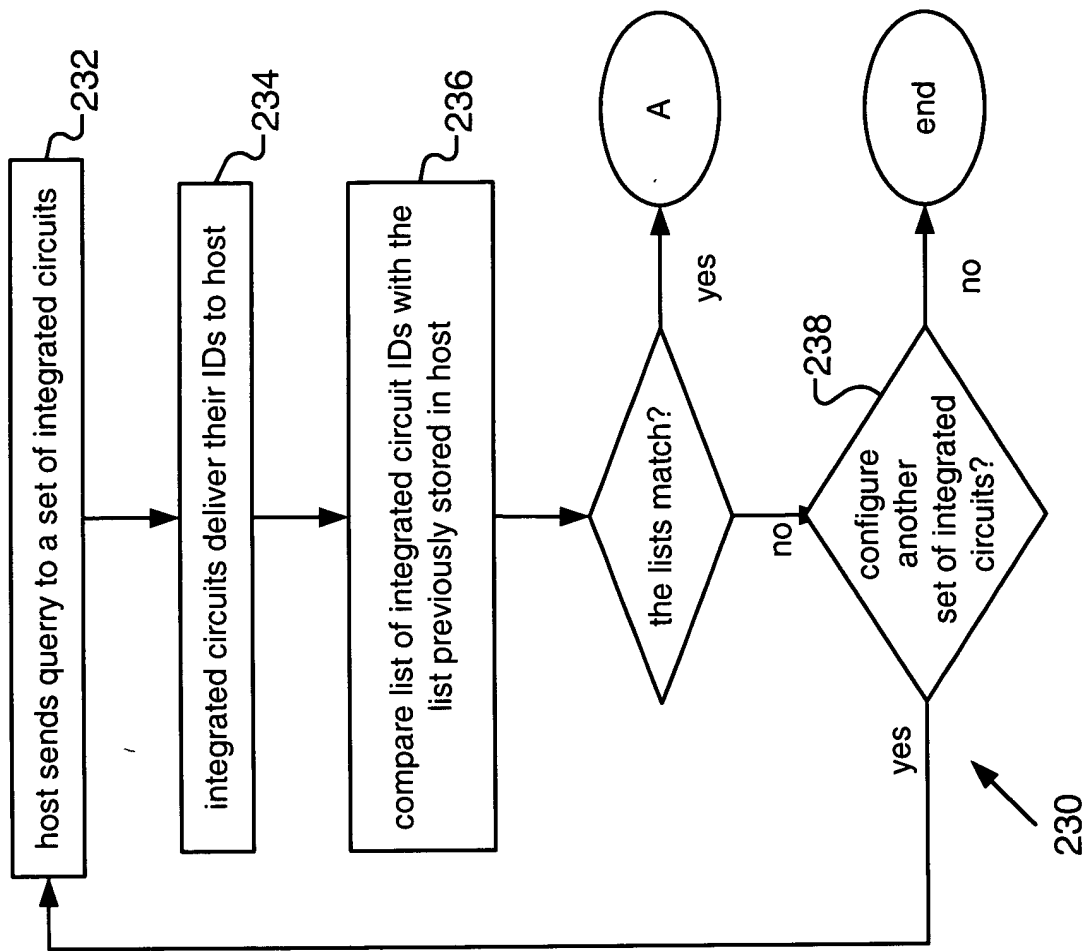


FIG. 5A

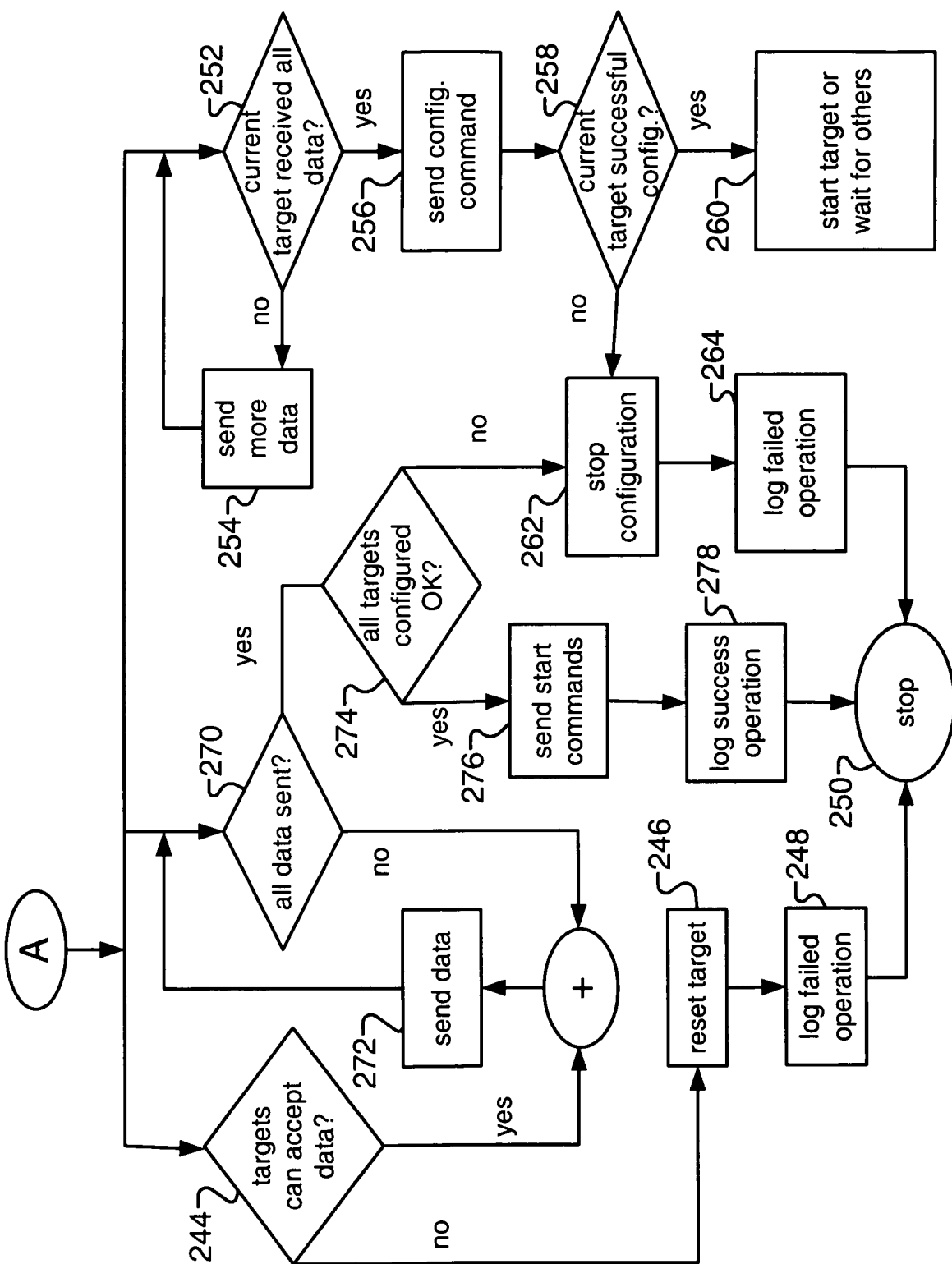


FIG. 5B

FIG. 6 is a block diagram of a system 300 including a wireless FPGA (master) 302, a first FPGA (slave) 304, and a second FPGA (slave) 306. The system 300 is configured to receive data from a data source (not shown) and output the data to a data destination (not shown). The system 300 includes a bus 308 that connects the three FPGAs. The bus 308 is configured to provide a common clock signal to the three FPGAs. The bus 308 is also configured to provide a common data path between the three FPGAs. The system 300 is configured to receive data from the data source and output the data to the data destination via the bus 308.

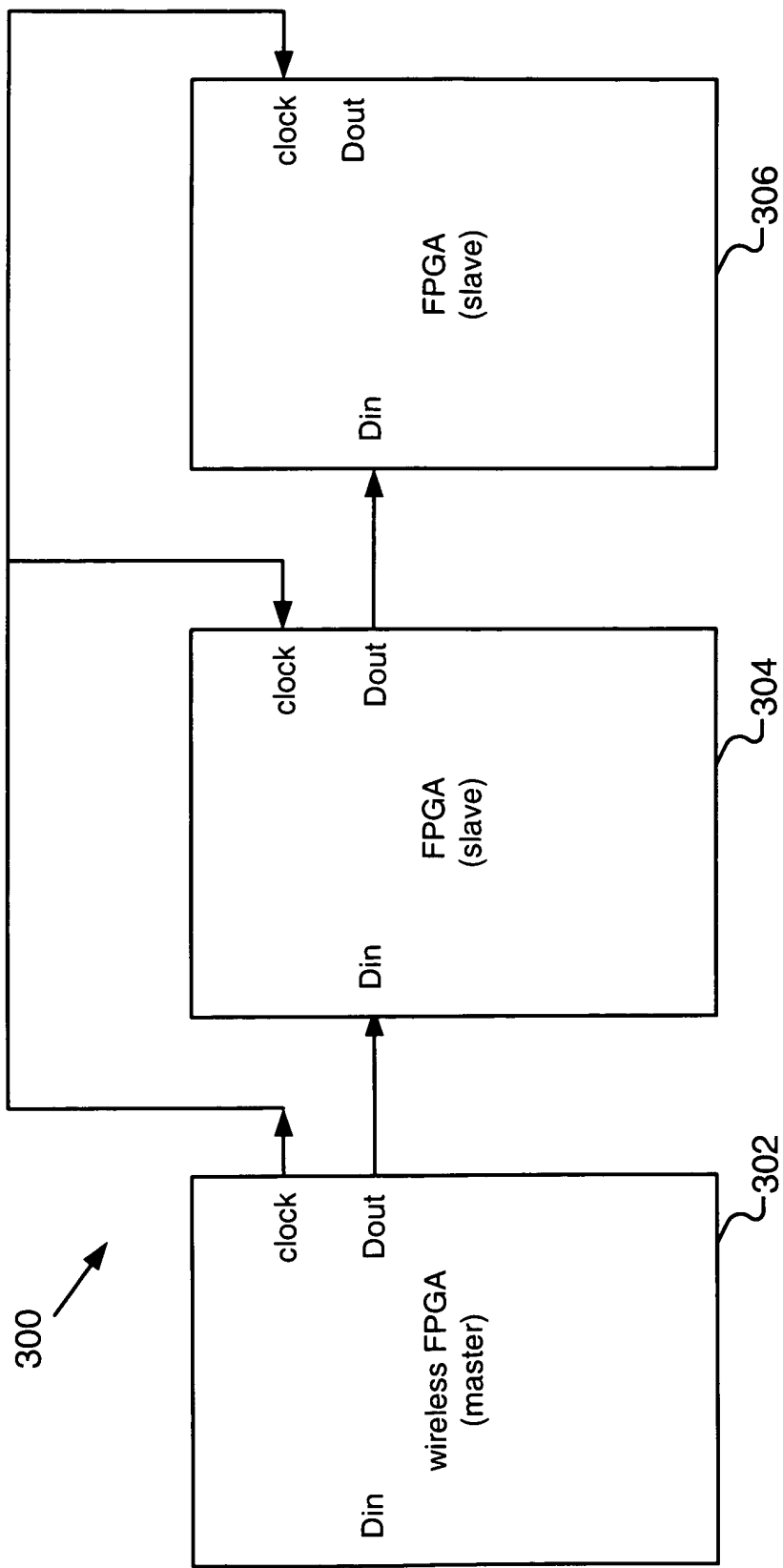


FIG. 6